

CLAIMS

What is claimed is:

- 1 1. An MRAM cell comprising:
 - 2 a magnetic tunneling junction including
 - 3 a free layer,
 - 4 a pinned layer, and
 - 5 a spacer layer disposed between the free layer and the pinned layer;
 - 6 a digit line including a bit line segment disposed proximate to the magnetic
 - 7 tunneling junction;
 - 8 a bit line including a bit line segment in electrical contact with the magnetic
 - 9 tunneling junction; and
 - 10 a magnetic liner layer disposed around the bit line segment and contacting the free
 - 11 layer.
- 1 2. The MRAM cell of claim 1 wherein the digit line segment is disposed proximate to
 - 2 the pinned layer and the bit line segment is in electrical contact with the free
 - 3 layer.
- 1 3. The MRAM cell of claim 1 wherein the bit line segment is disposed proximate to the
 - 2 pinned layer and the digit line segment is in electrical contact with the free layer.
- 1 4. The MRAM cell of claim 1 wherein the magnetic liner layer is electrically conductive.

- 1 5. The MRAM cell of claim 1 wherein the bit and digit lines are formed of a metal
2 selected from the group consisting of Cu, W, and Al.
- 1 6. The MRAM cell of claim 1 further including an antiferromagnetic layer disposed
2 adjacent to the pinned layer.
- 1 7. The MRAM cell of claim 1 wherein the magnetic liner layer is formed of Permalloy.
- 1 8. The MRAM cell of claim 7 wherein the Permalloy is between 16 and 22 atomic
2 percent iron.
- 1 9. The MRAM cell of claim 7 wherein the Permalloy is $\text{Ni}_{81}\text{Fe}_{19}$.
- 1 10. The MRAM cell of claim 1 wherein the magnetic liner layer has a thickness of about
2 20\AA to about 500\AA .
- 1 11. The MRAM cell of claim 1 wherein the magnetic liner layer has a thickness of about
2 30\AA to about 100\AA .
- 1 12. The MRAM cell of claim 1 wherein the magnetic liner layer is formed of a material
2 selected from the group consisting of CoZrCr, CoZrNb, CoZrRe, FeSiAl, FeN,
3 FeAlN, FeRhN, and FeTaN.

1 13. The MRAM cell of claim 1 wherein the pinned layer is two ferromagnetic layers
2 separated by a spacer layer.

1 14. The MRAM cell of claim 1 wherein the free layer is two ferromagnetic layers.

1 15. An MRAM cell comprising:

2 a magnetic tunneling junction including

3 a free layer having a magnetization orientation,

4 a pinned layer, and

5 an insulating spacer layer disposed between the free layer and the pinned
6 layer;

7 a digit line including a segment disposed proximate to the pinned layer;

8 a bit line including a segment in electrical contact with the free layer;

9 a magnetic liner layer disposed around the bit line segment and contacting the free
10 layer such that a magnetic field encircles the bit line segment.

1 16. The MRAM cell of claim 15 wherein the magnetic liner layer is electrically
2 conductive.

1 17. The MRAM cell of claim 15 wherein the bit and digit lines are formed of a metal
2 selected from the group consisting of Cu, W, and Al.

1 18. The MRAM cell of claim 15 further including an antiferromagnetic layer disposed
2 adjacent to the pinned layer.

1 19. The MRAM cell of claim 15 wherein the magnetic liner layer is formed of
2 Permalloy.

1 20. The MRAM cell of claim 19 wherein the Permalloy is between 16 and 22 atomic
2 percent iron.

1 21. The MRAM cell of claim 19 wherein the Permalloy is $\text{Ni}_{81}\text{Fe}_{19}$.

1 22. The MRAM cell of claim 15 wherein the magnetic liner layer has a thickness of
2 about 20Å to about 500Å.

1 23. The MRAM cell of claim 15 wherein the magnetic liner layer has a thickness of
2 about 30Å to about 100Å.

1 24. The MRAM cell of claim 15 wherein the pinned layer is two ferromagnetic layers
2 separated by a spacer layer.

1 25. The MRAM cell of claim 15 wherein the free layer is two ferromagnetic layers.

1 26. An MRAM cell comprising:
2 a magnetic tunneling junction including
3 a free layer,
4 a pinned layer, and
5 an insulating spacer layer disposed between the free layer and the pinned
6 layer;
7 a digit line including a segment disposed proximate to the pinned layer, the digit
8 line segment having a long axis defining a first direction;
9 an electrically insulating spacer layer disposed between the digit line segment and
10 the pinned layer;
11 a bit line including a segment in electrical contact with the free layer, the bit line
12 segment having a long axis defining a second direction substantially
13 perpendicular to the first direction;
14 a magnetic liner layer disposed around the bit line segment and contacting the free
15 layer.

1 27. The MRAM cell of claim 26 wherein the magnetic liner layer is electrically
2 conductive.

1 28. The MRAM cell of claim 26 wherein the bit and digit lines are formed of a metal
2 selected from the group consisting of Cu, W, and Al.

1 29. The MRAM cell of claim 26 further including an antiferromagnetic layer disposed
2 adjacent to the pinned layer.

1 30. The MRAM cell of claim 26 wherein the magnetic liner layer is formed of
2 Permalloy.

1 31. The MRAM cell of claim 30 wherein the Permalloy is between 16 and 22 atomic
2 percent iron.

1 32. The MRAM cell of claim 30 wherein the Permalloy is $\text{Ni}_{81}\text{Fe}_{19}$.

1 33. The MRAM cell of claim 26 wherein the magnetic liner layer has a thickness of
2 about 20Å to about 500Å.

1 34. The MRAM cell of claim 26 wherein the magnetic liner layer has a thickness of
2 about 30Å to about 100Å.

1 35. The MRAM cell of claim 26 wherein the pinned layer is two ferromagnetic layers
2 separated by a spacer layer.

1 36. The MRAM cell of claim 26 wherein the free layer is two ferromagnetic layers.

1 37. An MRAM cell comprising:
2 a magnetic tunneling junction including
3 a free layer,
4 a pinned layer, and
5 an insulating spacer layer disposed between the free layer and the pinned
6 layer;
7 a digit line including a segment disposed proximate to the pinned layer, the
8 segment having a long axis defining a first direction;
9 a bit line including
10 a segment in electrical contact with the free layer and having
11 a long axis defining a second direction substantially perpendicular
12 to the first direction,
13 a bottom surface abutting the free layer,
14 a top surface opposite the bottom surface, and
15 first and second vertical surfaces opposite one another and
16 connecting the top and bottom surfaces; and
17 a magnetic liner layer disposed around the bit line segment and contacting the
18 first and second vertical surfaces and the top surface.

1 38. The MRAM cell of claim 37 wherein the magnetic liner layer also contacts the free
2 layer.

1 39. The MRAM cell of claim 37 wherein the magnetic liner layer is electrically
2 conductive.

1 40. The MRAM cell of claim 37 wherein the bit and digit lines are formed of a metal
2 selected from the group consisting of Cu, W, and Al.

1 41. The MRAM cell of claim 37 further including an antiferromagnetic layer disposed
2 adjacent to the pinned layer.

1 42. The MRAM cell of claim 37 wherein the magnetic liner layer is formed of
2 Permalloy.

1 43. The MRAM cell of claim 42 wherein the Permalloy is between 16 and 22 atomic
2 percent iron.

1 44. The MRAM cell of claim 42 wherein the Permalloy is $\text{Ni}_{81}\text{Fe}_{19}$.

1 45. The MRAM cell of claim 37 wherein the magnetic liner layer has a thickness of
2 about 20Å to about 500Å.

1 46. The MRAM cell of claim 37 wherein the magnetic liner layer has a thickness of
2 about 30Å to about 100Å.

1 47. The MRAM cell of claim 37 wherein the pinned layer is two ferromagnetic layers
2 separated by a spacer layer.

1 48. The MRAM cell of claim 37 wherein the free layer is two ferromagnetic layers.

1 49. An MRAM cell comprising:

2 a magnetic tunneling junction including

3 a free layer,

4 a pinned layer, and

5 an insulating spacer layer disposed between the free layer and the pinned
6 layer;

7 a digit line including a segment disposed proximate to the pinned layer, the digit
8 line segment having a long axis defining a first direction;

9 a bit line including a bit line segment in electrical contact with the free layer and
10 having a long axis defining a second direction substantially perpendicular
11 to the first direction; and

12 a magnetic sheath disposed around the bit line segment and formed from the free
13 layer and a magnetic liner layer.

1 50. The MRAM cell of claim 49 wherein the magnetic liner layer is electrically
2 conductive.

- 1 51. The MRAM cell of claim 49 wherein the bit and digit lines are formed of a metal
2 selected from the group consisting of Cu, W, and Al.
- 1 52. The MRAM cell of claim 49 further including an antiferromagnetic layer disposed
2 adjacent to the pinned layer.
- 1 53. The MRAM cell of claim 49 wherein the magnetic liner layer is formed of
2 Permalloy.
- 1 54. The MRAM cell of claim 53 wherein the Permalloy is between 16 and 22 atomic
2 percent iron.
- 1 55. The MRAM cell of claim 53 wherein the Permalloy is $\text{Ni}_{81}\text{Fe}_{19}$.
- 1 56. The MRAM cell of claim 49 wherein the magnetic liner layer has a thickness of
2 about 20Å to about 500Å.
- 1 57. The MRAM cell of claim 49 wherein the magnetic liner layer has a thickness of
2 about 30Å to about 100Å.
- 1 58. The MRAM cell of claim 49 wherein the pinned layer is two ferromagnetic layers
2 separated by a spacer layer.

1 59. The MRAM cell of claim 49 wherein the free layer is two ferromagnetic layers.

1 60. A method of fabricating an MRAM cell comprising:

2 providing a substrate;

3 forming a digit line on the substrate;

4 forming an insulating spacer including a contact via over the bit line;

5 forming a bottom lead over the insulating spacer;

6 forming a magnetic tunnel junction stack over the bottom lead;

7 forming a first liner layer over the magnetic tunnel junction;

8 forming a bit line over the magnetic tunnel junction stack; and

9 forming a second liner layer over the bit line.

1 61. The method of claim 60 wherein forming the bit line includes

2 forming and patterning an oxide layer on the substrate;

3 depositing a conductive metal; and

4 planarizing a top surface of the conductive metal.

1 62. The method of claim 61 wherein the conductive metal is selected from the group

2 consisting of copper, tungsten, and aluminum.

1 63. The method of claim 61 wherein planarizing is performed by CMP.

1 64. The method of claim 60 wherein forming the bottom lead is performed by depositing
2 a conductive metal selected from the group consisting of copper, tungsten, and
3 aluminum.

1 65. The method of claim 60 wherein forming the bottom lead includes a patterning step.

1 66. The method of claim 60 wherein forming the magnetic tunnel junction stack includes
2 forming a first ferromagnetic layer over the bottom lead;
3 forming a tunneling barrier layer over the first ferromagnetic layer; and
4 forming a second ferromagnetic layer over the tunneling barrier layer.

1 67. The method of claim 66 wherein forming the magnetic tunnel junction stack further
2 includes forming an antiferromagnetic layer between the first ferromagnetic layer
3 and the bottom lead.

1 68. The method of claim 66 wherein forming the magnetic tunnel junction stack further
2 includes forming an antiferromagnetic above the second ferromagnetic layer.

1 69. The method of claim 66 wherein forming the magnetic tunnel junction stack further
2 includes a patterning step.

1 70. The method of claim 60 further comprising forming an insulating material layer over
2 the insulating spacer.

- 1 71. The method of claim 70 wherein forming an insulating material layer includes
2 forming a trench therein and over the magnetic tunnel junction stack.
- 1 72. The method of claim 71 wherein the trench has first and second sidewalls.
- 1 73. The method of claim 72 wherein the first liner layer is formed on the first and second
2 sidewalls.
- 1 74. The method of claim 60 wherein the first liner layer is formed with a thickness in the
2 range of about 20Å to about 500Å.
- 1 75. The method of claim 60 wherein the first liner layer is formed by ion beam
2 deposition or physical vapor deposition.
- 1 76. The method of claim 60 wherein the first liner layer is formed of Permalloy.
- 1 77. The method of claim 60 further comprising forming a stop layer over the first liner
2 layer.
- 1 78. The method of claim 77 further comprising forming a seed layer over the stop layer.
- 1 79. The method of claim 60 wherein forming the bit line includes forming a seed layer.

1 80. The method of claim 60 wherein the bit line is formed of a conductive metal selected
2 from the group consisting of copper, tungsten, and aluminum.

1 81. The method of claim 60 wherein forming the bit line includes a planarization.

1 82. The method of claim 81 wherein forming the bit line includes an ion beam etch.

1 83. The method of claim 60 wherein forming the second liner layer includes
2 forming and patterning a mask; and
3 removing portions of the second liner layer.

1 84. The method of claim 60 wherein the second liner layer is formed with a thickness in
2 the range of about 20Å to about 500Å.

1 85. The method of claim 60 wherein the second liner layer is formed of Permalloy.

1 86. A method of fabricating an MRAM cell comprising:
2 providing a digit line;
3 forming a magnetic tunnel junction stack over the digit line;
4 forming a bit line; and
5 forming a magnetic liner layer over the bit line and in contact with the magnetic
6 tunnel junction stack.

1 87. The method of claim 86 wherein forming a magnetic tunnel junction stack includes
2 forming a free ferromagnetic layer and wherein the magnetic liner layer is formed
3 in contact with the free ferromagnetic layer.

1 88. A method of storing a bit of data in an MRAM cell, comprising:
2 pinning a magnetic orientation of a first ferromagnetic layer in a magnetic tunnel
3 junction;
4 simultaneously generating
5 a first write current in a digit line including segment proximate to the
6 magnetic tunnel junction and
7 a second write current in a bit line including segment proximate to the
8 magnetic tunnel junction, the write currents being sufficient to
9 produce a magnetic field capable of orienting a magnetic domain
10 of a second ferromagnetic layer in the magnetic tunnel junction;
11 and
12 maintaining the orientation of the magnetic field of the second ferromagnetic
13 layer by creating a magnetic loop around the bit line.